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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE					ATTY. DOCKET NO. PU020001		SERIAL NO.	
INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 (Use several sheets if necessary)					APPLICANTS LOUIS ROBERT LITWIN, JR. ET AL.			
					FILING DATE HEREWITH		GROUP	
U.S. PATENT DOCUMENTS								
EXAMINE INITIAL		DOCUMENT NUMBER	ISSUE DATE	APPLICANT/PATENTEE	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE	
	AA	4,875,211	10/17/89	K. Murai et al.	371	40.1		
	AB	5,373,511	12/13/94	I. E. Veksler	371	37.4		
	AC	6,058,500	05/02/00	P. A. DesJardins et al.	714	781		
	AD	6,061,826	05/09/00	H. Thirumoorthy et al.	714	784		
	AE	6,065,149	05/16/00	R. Yamanaka	714	780		
	AF	6,175,945	01/16/01	S. Okita	714	784		
	AG	6,195,781	02/27/01	S. Kosuge	714	784		
	AH							
	AI							
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	PUBL. DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION Yes No	
	AL							
	AM							
	AN							
	AO							
	AP							
	AQ							
OTHER INFORMATION (Including Author, Title, Pub.Date, Pertinent Pages, Country, Etc.)								
	AR	"Quantum Reed - Solomon Codes", Markus Grassl, Willi Geiselmann, and Thomas Beth, Institut für Algorithmen und Kognitive Systeme, Arbeitsgruppe Quantum Computing, Universität Karlsruhe, Am Fasanengarten 5, 76 128 Karlsruhe, Germany, pp. 1-14.						
	AS	"Optimal Finite Field Multipliers for FPGAs", Captain Gregory C. Ahlquist, Brent Nelson, and Michael Rice, article found at http://splash.ee.byu.edu/docs/ffmult.fpl99.pdf - Similar pages, 3/1/2001, 10 pages.						
	AT	"Tutorial on Reed-Solomon Error Correction Coding", William A. Geisel, NASA Technical Memorandum 102162, August 1990, pp. 72-74.						
EXAMINER					DATE CONSIDERED			
SUBMITTED BY:					REG.NO.:		DATE:	
GUY H. ERIKSEN					41,736		January 23, 2002	

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OTHER INFORMATION (Including Author, Title, Pub.Date, Pertinent Pages, Country, Etc.)		
AR		"ERROR CONTROL SYSTEMS for Digital Communication and Storage", Stephen B. Wicker, Library of Congress Cataloging-in-Publication Data, p. 209.
AS		"Parallel Decoder for Cellular Automata Based Byte Error Correcting Code", S. Chattopadhyay and P. Pal Chaudhuri, 10th International Conference on VLSI Design, January 1997, pp. 527-528.
AT		"Designing a Reed-Solomon Codec in an ADSL System using a C6201 DSP", by Han Kuo, article found, at http://www.csdmag.com/news/des0111011.htm , 3/9/01, 10 pages.

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OTHER INFORMATION (Including Author, Title, Pub.Date, Pertinent Pages, Country, Etc.)		
AR		"A Faster Way To Run Reed Solomon Decoders", Torjell Berg and Aaron Brennan, American Microsystems Inc., Article found at http://www.eetasia.com/article_content.php3?article_id=8800067078 3/9/01; posted: 01 Jan 2001, 3 pages.
AS		"XF-RSDEC Reed Solomon Decoder", article found at http://www.xilinx.com/products/logiccore/alliance/memec/xf_rsdec.pdf , January 10, 2000, pp. 3-1 - 3-5.
AT		"REED-SOLOMON CODES - 'An introduction to Reed-Solomon codes: principles, architecture and implementation'", article found at http://www.4i2i.com/reed_solomon_codes.htm , 3/9/01, 8 pages.

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OTHER INFORMATION (Including Author, Title, Pub.Date, Pertinent Pages, Country, Etc.)			
AR		"Reed Solomon Decoder: TMS320C64x Implementation, 'Digital Signal Processing Solutions', Jagadeesh Sankaran, TEXAS INSTRUMENTS Application Report SPRA686 - December 2000, pp. 1-20, 31, 38, 49, 60, 67-70.	
AS			
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